LSI DOCKET NO. 01-304

CLAIMS:

What is claimed is:

1. An electro-static discharge device having connections to a pad and a substrate, said electro-static discharge device comprising:

a diode coupled for providing a bias signal, having a cathode coupled to said pad and an anode coupled to said substrate; and

a transistor operating in response to said bias signal, said transistor having a drain terminal coupled to said pad, a source terminal coupled to said substrate, and a gate terminal coupled to said substrate and to said source terminal.

2. The electro-static discharge device of claim 1, further comprising a substrate resistor having a first conduction terminal coupled to said gate terminal of said transistor and said source terminal of said transistor, and a second conduction terminal coupled to said substrate.

3. The electro-static discharge device of claim 1, wherein the substrate is coupled to receive a ground reference potential and comprises a material having a first conductivity type and a first doping concentration, and the anode of the diode comprises a material having the first conductivity type and a second doping concentration that is greater than the first doping concentration.

4. The electro-static discharge device of claim 3, wherein the drain of the transistor, the source of the transistor, and the cathode of the diode comprise a material with a second conductivity type that is opposite in polarity to the first conductivity type.

5. The electro-static discharge device of claim 1, wherein the diode comprises a MOS diode coupled for providing the bias signal to the gate terminal of the transistor in response to a pad voltage that is greater than an operating voltage.

6. The electro-static discharge device of claim 1, wherein the diode comprises a zener diode coupled for providing a bias signal to the gate terminal of the transistor in response to a pad voltage that is greater than an operating voltage.

7. The electro-static discharge device of claim 1, wherein the transistor, operating in response to the bias signal from the diode, is coupled for conducting a current from the pad to the substrate.

8. The electro-static discharge device of claim 1, wherein said transistor is a MOSFET.

9. A semiconductor device having a pad and a substrate, comprising:

a diode coupled for providing a bias signal, said diode having a first conduction terminal coupled to said pad and a second conduction terminal coupled to said substrate.

a transistor operating in response to said bias signal, said transistor having a first conduction terminal coupled to said pad, a second conduction terminal coupled to said substrate, and a control terminal coupled to said second conduction terminal and to said substrate.

10. The semiconductor device of claim 9, further comprises a substrate resistor having a first conduction terminal coupled to said control terminal of said transistor and said second conduction terminal of said transistor, and a second conduction terminal coupled to said substrate.

11. The semiconductor device of claim 9, wherein said transistor, operating in response to said bias signal from said diode, is coupled for conducting a current from said pad to said substrate.

12. The semiconductor device of claim 11, wherein said transistor comprises a Metal Oxide Semiconductor field effect transistor having a gate terminal coupled for receiving said bias signal.

13. The semiconductor device of claim 11, wherein said transistor is an N-type MOSFET.

14. The semiconductor device of claim 9, wherein said diode comprises a zener diode coupled for providing said bias signal to said control terminal of said transistor in response to a pad voltage that is greater than an operating voltage.

15. The semiconductor device of claim 9, wherein said diode comprises an MOS diode coupled for providing said bias signal to said control terminal of said transistor in response to a pad voltage that is greater than an operating voltage.

16. A semiconductor chip package comprising

a semiconductor chip having a substrate thereof electrically tied to ground; and

an electrical connector configured to carry a supply voltage to said semiconductor chip;

wherein said semiconductor chip contains an electrostatic discharge device comprises

a diode coupled for providing a bias signal, said diode having a first conduction terminal coupled to said electrical connector and a second conduction terminal coupled to said substrate; and

a transistor operating in response to said bias signal, said transistor having a first conduction terminal coupled to said electric connector, a second conduction terminal coupled to said substrate, and a control terminal coupled to said second conduction terminal and to said substrate.

17. A method of protecting a semiconductor device, comprising:

detecting a first signal that is greater than a second signal; and

conducting said first signal into a substrate that is coupled to receive a ground reference potential upon detecting said first signal.

18. The method of claim 17, wherein detecting said first signal comprises:

conducting a current of said first signal through a diode; and

providing a control signal to a control terminal of a transistor in response to conducting said current.

19. The method of claim 17, wherein conducting said first signal comprises:

receiving a control signal at a control terminal of a transistor; and

converting said first signal into a current with a substrate resistor that is coupled to the substrate, thereby conducting the first signal into the substrate.

20. A method of making an electrostatic discharge semiconductor device on a semiconductor substrate having a first conductivity type and a first doping concentration, comprising:

implanting into the substrate first, second, and third well regions having second conductivity types that are opposite in polarity to said first conductivity type;

implanting a fourth well region of the first conductivity type adjacent to said substrate and adjacent to said first well region; and

forming an insulated terminal across said second and said third well regions.

21. The method of claim 20, further comprising implanting a fifth well region into said substrate having the first conductivity type and a second doping concentration.

22. The method of claim 20, wherein implanting said fourth well comprises doping the fourth well region with a second doping concentration that is greater than the first doping concentration.

23. The method of claim 20, further comprising forming an insulated terminal above said first well region.

24. The method of claim 20, wherein said fourth well region comprises a halo region adjacent to said first well region that reduces a breakdown voltage between the first well region to the substrate.

25. The method of claim 20, wherein the fourth well region comprises forming a lightly doped drain adjacent to said first well region that reduces a breakdown voltage between said first well region to said substrate.

26. The method of claim 20, wherein said fourth well region is adjacent to said second well region that reduces a breakdown voltage between said first well region to said substrate.